REMARKS

Claims 1-20 are pending in this application, of which claims 3-6, 8, 10, 12, 14, and 16-20 are withdrawn from consideration.

§ 103(a) Rejection of Claims 1, 2, 7, 9, 11, 13, and 15 over *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.*

Applicants respectfully traverse the rejection of claims 1, 2, 7, 9, 11, 13, and 15 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,994,762 to Suwanai et al. ("*Suwanai et al.*") in view of *Wolf et al.*, and further in view of U.S. Patent No. 6,770,977 to Kishida et al. ("*Kishida et al.*"). A *prima facie* case of obviousness has not been established.

"Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 at 17-18 (1966).

"[T]he analysis supporting a rejection ... should be made explicit" and it is "important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements in the manner claimed." *USPTO Memorandum* from Margaret A. Focarino, Deputy Commissioner for Patent Operations,

May 3, 2007, page 2 (citing *KSR Int'l Co. v. Teleflex, Inc.*, No. 04-1350 (U.S. Apr. 30, 2007)).

Suwanai et al. teaches a semiconductor integrated circuit device. As shown in Figure 11, the device has a "BPSG [(boron-doped phospho silicate glass)] film 17 and a silicon oxide film 27" (col. 7, line 66 to col. 8, line 2) that has been "deposited ... on the BPSG film 17" (col. 10, lines 21-22). "Further, a wiring 18 constituting a portion of the guard ring GR is formed on the silicon oxide film 27 at the outer circumference of the chip" (col. 8, lines 2-4). The device also has another "BPSG film 20" (col. 8, lines 25-27) and an "interlayer insulation film 23" (col. 8, line 49).

Wolf et al. teaches: "Interconnect delay can be reduced not only by decreasing R of the conductor structures in ICs, but also by decreasing C of the dielectric layers. The value of C, in turn, can be reduced by using dielectric materials with smaller permittivity values (i.e., *low-k dielectric materials*)" (pg. 791, paragraph 1). "[U]ltra-low *k* dielectric materials were ... being investigated for their suitability as IC interconnect layers" (pg. 794, paragraph 6).

Kishida et al. teaches, referring to Figures 7A, 7B, 8A, and 8B, that "a barrier layer composed of a first tantalum nitride film 202 and a first β-tantalum film 203 ... is formed on the bottom and the walls of [an] interconnect groove of [an] insulating film 201. Then, after forming a first copper seed layer 204 on the first β-tantalum film 203, the first copper seed layer 204 is grown through the electroplating, so as to form a first copper plating layer 205." (Col. 8, lines 23-35.)

Even if each and every element of independent claim 1, from which claims 2, 7, 9, 11, 13, and 15 depend, could be found in *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.*, which Applicants do not concede, it would not have been obvious to combine the references as suggested by the Examiner because *Suwanai et al.* teaches away from combining the references to obtain the semiconductor device recited in claim 1. "[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR* at 12 (citing *United States v. Adams*, 383 U.S. 39, 51–52 (1966)).

The Examiner alleges that a relative dielectric constant of over 3.8 is an inherent property of the BPSG films (17, 20) of *Suwanai et al.* (Office Action, page 3, paragraph 1). The Examiner further alleges, "[i]t would have been obvious to one of ordinary skill ... to use a low k dielectric material (e.g. nanoporous silica SiO_2) having a dielectric constant of less than 2.0 for the first dielectric layer disclosed by Suwanai in order to reduce the interconnect delay as taught by Wolf and to include a barrier layer on an outer surface [of] a conductor layer disclosed by Suwanai in view of Wolf to prevent the metal atoms of the conductive layer from diffusing into the semiconductor substrate" (Office Action, page 4, paragraph 1.)

Suwanai et al. teaches away from combining the references as suggested by the Examiner because *Suwanai et al.* teaches forming each of the insulating films (20, 23, 17, and 27) both inside the guard ring (GR) and outside the guard ring simultaneously. Applicants note that the guard ring is formed to be buried into an etched trench in the insulating films (20, 23, 17, and 27). Therefore, using a low-k dielectric material with a

dielectric constant of less than 2.0 for any of the layers (20, 23, 17, and 27) of *Suwanai et al.*, as suggested by the Examiner, would result in those layers (20, 23, 17, and 27) having a dielectric constant of 3.8 or less at locations both inside and outside of the guard ring. Thus, *Suwanai et al.* teaches away from combining the references to form the insulating films (20, 23, 17, and 27) inside the guard ring separately from forming the insulating films (20, 23, 17, and 27) outside the guard ring to obtain a semiconductor device comprising, inter alia, "a first insulating film ... having a relative dielectric constant of 3.8 or less; a conductor which covers a side face of the first insulating film ...; and a second insulating film covering the outer side face of the conductor and having a relative dielectric constant of over 3.8," as recited in claim 1.

Furthermore, one of ordinary skill would not have been motivated to combine the references as suggested by the Examiner because one of ordinary skill would understand that forming the insulating films (20, 23, 17, and 27) outside the guard ring to have a relative dielectric constant of 3.8 or less would make these insulating films (20, 23, 17, and 27) susceptible to damage from cracking or peeling outside the guard ring when the semiconductor wafer is diced.

Thus, since it would not have been obvious to one of ordinary skill to combine *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* to obtain the semiconductor device recited in claim 1, claim 1 and claims 2, 7, 9, 11, 13, and 15, which depend therefrom, are allowable over *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* under § 103(a).

CONCLUSION

In view of the foregoing remarks, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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